CSRCompiler

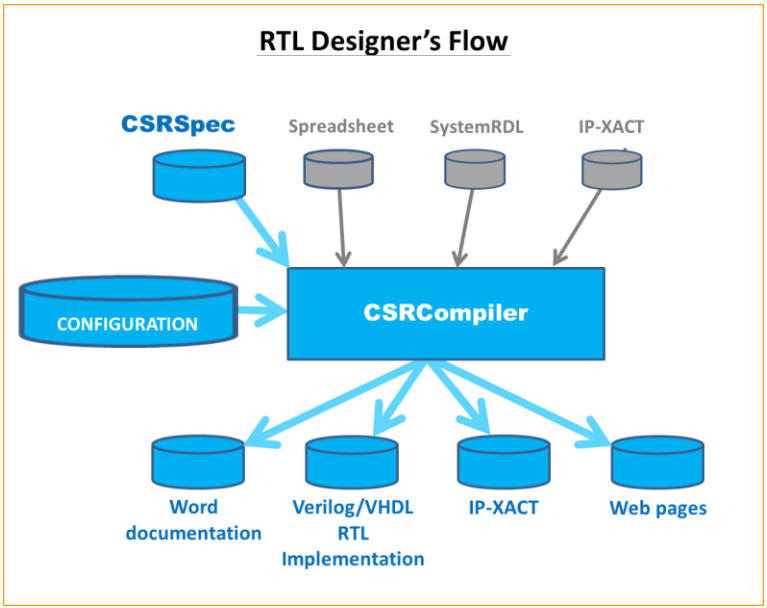
The complete single source for Address Maps

Semifore's CSRCompiler™ and CSRSpec™ language are a complete register design solution for hardware, software, verification and documentation. Collaboratively manage your design from a single source specification. CSRCompiler turns address map sharing into a smooth, integrated process. Only Semifore gives your entire team a complete, correct, up to date register design ecosystem.

Raising Register Standards

CSRCompiler is a true status and control register compiler developed by engineers with years of both software and hardware register experience. It is currently in use in the Mil/Aero, Communications, Semiconductor,and Medical industries by companies such as Microsoft, Altera, Northrop Grumman, LSI, and Applied Micro Circuits Corporation.

CSRCompiler is the only register tool that detects both design function and semantic problems. Preventing design mistakes during address map deployment is critical when trying to include 3rd-party IP cores. Unlike scripts, CSRCompiler generates a complete data design structure which is analyzed for validity before being used to create hardware designs verification, software headers and documentation.



INPUTS:

- ✓ CSRSpec Language
- ✓ SPIRIT SystemRDL
- ✓ IEEE 1685 IP-XACT XML
- ✓ CMSIS-SVD
- ✓ Excel® Spreadsheets
- ✓ VMM RALF
- ✓ Legacy Input Languages

OUTPUTS:

Synthesizable RTL

CSRCompiler generates the synthesizable Verilog® and VHDL code for configuration, status, interrupts, masks, counters, and other memory-map registers. The synthesizable Verilog® code for standard configuration registers can jump start your design. Synthesizable standard bus interfaces, AMBA®, Avalon®, OCP-IP and Wishbone aid in IP integration for multi-core and embedded architectures.

Dynamic HTML Web Pages

CSRCompiler automatically generates a HTML interactive view for browsing the entire design.

Headers for Firmware

CSRCompiler builds the headers for firmware code. Semifore's single source eliminates the chance of typos and missing parameters.

Data Structures

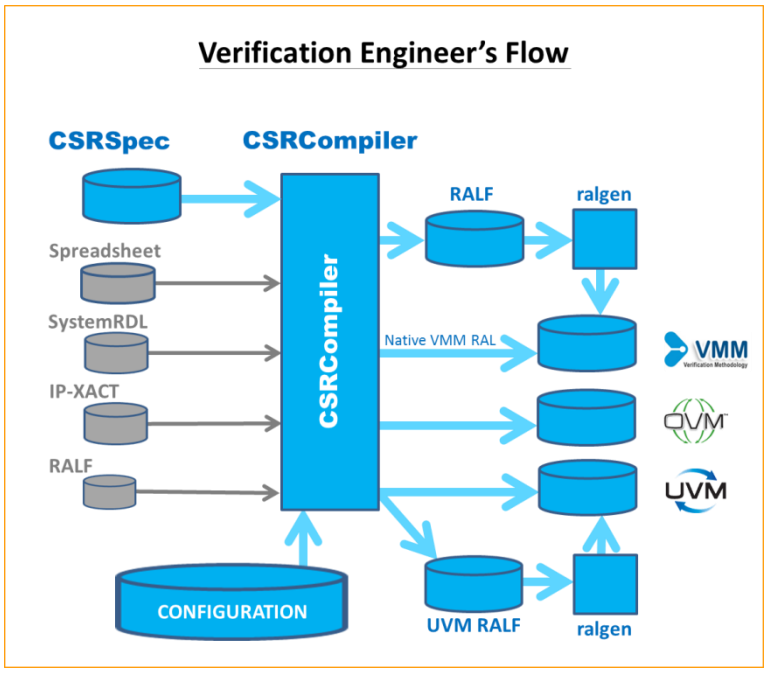
CSRCompiler generates the SystemVerilog, C/C++, and Perl data structures to jump start system and unit testing of memory-map registers. Semifore also supports UVM, VMM and OVM for design verification. IEEE 1685 IP-XACT XML is provided for interchange. The registers are specified once, and, all the views are generated by CSRCompiler ensuring that they are accurate as the design evolves.

Internal and Customer Documentation

Formatted documentation views provide a clean handoff from design to technical publication. Semifore's single source eliminates the risk of "stale specifications". Word©, Framemaker® and DocBook XML are all supported.

VERIFICATION

As a member of the Accellera VIP Technical Committee, Semifore leads the industry in fully supporting the UVM register class library. Semifore's CSRCompiler automatically generates UVM register class definitions directly from any of the following formats: CSRSpec, SPIRIT SystemRDL, IEEE 1685 IP-XACT, VMM RALF, and spreadsheet.



CSRCOMPILER

- ✓ Saves the verification team significant time when creating register class definitions.
- ✓ Eliminates the possibility of introducing verification errors by removing the need for manual data entry.
- ✓ Guarantees your team is accessing the most recent control and status information. A changed field position within a register or a modified register address will no longer cause a long, overnight regression to fail.

CSRCompiler generates the following –

- ✓ **UVM register class definitions:** CSRCompiler generates the UVM System Verilog class definitions for the control and status registers based on the UVM register package. The register and its UVM class definition are always in sync.
- ✓ **Improved backdoor access for VMM:** CSRCompiler has capabilities beyond those of RALF/ralgen for specifying HDL paths.
- ✓ **Conversion from VMM RALF:** Semifore offers a conversion facility to translate VMM RALF files into CSRSpec, SPIRIT SystemRDL, IEEE 1685 IP-XACT or spreadsheet. This allows the easy importation of legacy designs.
- ✓ ***Verilog® and VHDL Header Files:*** Automatically-generated, extensive set of Verilog macro or VHDL constant definitions, indispensable for verifying the DUT. This ensures the verification team is always accessing the most up-to-date configuration and status register information.

ADVANCED CSRCOMPILER FEATURES

CSRCompiler's advanced features provide numerous benefits over homegrown scripts. Homegrown scripts often fall far short in providing accurate, complete, and consistently generated views of your large address map; views that are critical to all members of your team.

Feature	CSRCompiler	Homegrown scripts
Field / register cross referencing	✓	X
Time-saving template support	✓	X
Industry-standard buses	✓	X
Detects faulty 3rd-party IP cores	✓	X
Extensive error / syntax checking	✓	X
IEEE IP-XACT semantic consistency rule checks	✓	X
Hardware interrupt bit-enable support	✓	X
All features QA'd against large regression test suite	✓	?
Single source for generating RTL, DV, firmware & documentation	✓	X
UVM, OVM, VMM register class definitions	✓	X
Improved backdoor access for VMM	✓	X
Multiple domains support	✓	X
Large capacity (100,000 registers)	✓	?
High-speed (38sec / 10,000 registers)	✓	X
Virtual register files	✓	X

Contact us for details of our evaluation program:

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