Semifore

Total Register Automation

FEATURES AND FUNCTIONS

- Over 400 Configuration Properties
- **Over 1000 Error Checks**
- AMBA4 APB
- Customized C Header Outputs
- Union Objects
- Byte Access
- Field Compare
- Continuous Iteration flow
- Wide Memories
- Advanced Spreadsheet Features
- Extensive Math Checking
- Correct Data Model
- UVM-SystemC Output
- Coverage Bins
- Broadcast
- Parity Checks
- Back Door Path Mapping
- Port Arrays
- **SystemVerilog RTL**
- Cross Reference Capabilities
- Atomic Access for Wide Registers
- Register Alias and Broadcast Registers
- Virtual Registers
- Sharing of Objects and Registers
- Wide Register Support
- Correct Semantics
- **Linking All Formats**
- Correct Syntax
- 256K Data Path
- Bit Access
- Hierarchical Address Maps, Registers and Fields
- Parametrized Templates
- Internal and External Documentation Security
- Extensive Hierarchy Levels
- AXI BUS Protocol

BENEFITS AND SUPPORT

- **Over 6000 Register Behaviors**
- 1 Million Registers
- **Real Tools - Not Scripts**
- Highest Quality RTL
- Tier 1 Tape Outs
- **Seconds - Not Hours**
- Highly Configurable
- Highest Capacity Today
- **Break the Silos**
- Blazing Fast Performance
- Linting Standards Formats
- Linting 3rd-Party IP
- Built-In Design Expertise
- The Most Advanced Language
- The Universal Translator
- **True Cross Compiler**
- The Reference for SystemRDL
- Executable Specification
- Respond to Change
- Not Just a Transform Engine
- Lower Cost of Ownership
- Individuals and Interactions
- **“Iterate Iterate Iterate”**
- Improved Time to Tape Out
- No Scripting Required
- 30-day Evaluation to Production
- Sharing Data Quickly
- SCRUM for Productivity
- Agile Design Work Flow
- Designers Design vs. Scripting
- **Generate All Versions of IP-XACT**
- Single View of Meta Data
- Correct by Construction RTL
- Immediate Team Communication
- **Any Machine Readable Input**
- A Superset Language
- Industry Standard Buses
- Eliminate Translation Errors
- Combine Legacy and New Design Data