Semifore

Total Register Automation

# CSRCompiler

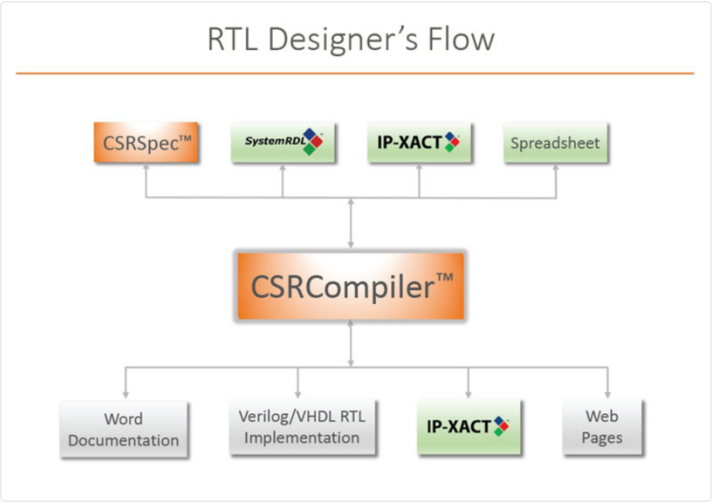
**The complete single source for Address Maps**

Semifore's CSRCompiler™ system and CSRSpec™ language are a complete register design solution for hardware, software, verification and documentation. Collaboratively manage your design from a single source specification. CSRCompiler turns address map sharing into a smooth, integrated process. Only Semifore gives your entire team a complete, correct, up to date register design ecosystem.

## Raising Register Standards

CSRCompiler is a true status and control register compiler developed by engineers with years of both software and hardware register experience. It is currently in use in the Aerospace, Communications & Networking, Semiconductor, Graphics and Medical industries.

CSRCompiler is the only register tool that detects both design function and semantic problems. Preventing design mistakes during address map deployment is critical when trying to include third-party IP cores. Unlike scripts, CSRCompiler generates a complete data design structure which is analyzed for validity before being used to create hardware designs, verification, software headers and documentation.




## Inputs

- CSRSpec Language
- SystemRDL
- IP-XACT
- CMSIS-SVD
- Excel® Spreadsheets
- VMM RALF
- Legacy Input Languages

## Outputs

### Synthesizable RTL

CSRCompiler generates the synthesizable Verrilog® and VHDL code for configuration, status, interrupts, masks, counters, and other memory map registers. The synthesizable Verilog code for standard configuration registers can jump-start your design. Synthesizable standard bus interfaces, AMBA®, Avalon®, OCP-IP and Wishbone aid in IP integration for multi-core and embedded architectures.

### Dynamic HTML Web Pages

CSRCompiler automatically generates the HTML interactive view for browsing the entire design.

### Headers for Firmware

CSRCompiler builds the headers for firmware code. Semifore's single source eliminates the chance of typos and missing parameters.

### Data Structures

CSRCompiler generates the SystemVerilog, C/C++ and Perl data structures to jump-start system and unit testing of memory map registers. Semifore also supports UVM, VMM and OVM for design verification. IP-XACT XML is provided for interchange. The registers are specified once, and all the views are generated by CSRCompiler ensuring that they are accurate as the design evolves.

### Internal and Customer Documentation

Formatted documentation views provide a clean handoff from design to technical publications. Semifore's single source eliminates the risk of "stale specifications". Word®, Framemaker® and DocBook XML are all supported.

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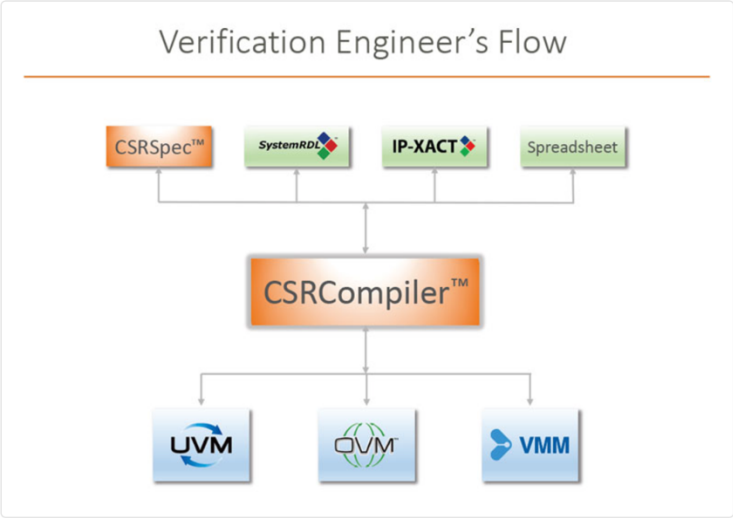
## Verification

As a member of the Accellera VIP Technical Committee, Semifore leads the industry in fully supporting the UVM register class library. Semifore's CSRCompiler automatically generates UVM register class definitions directly from any of the following formats: CSRSpec, SystemRDL, IP-XACT, VMM RALF and spreadsheet.




### CSRCompiler

- Saves the verification team significant time when creating register class definitions
- Eliminates the possibility of introducing verification errors by removing the need for manual data entry
- Guarantees your team is accessing the most recent control and status information. A changed field position within a register or a modified register address will no longer cause a long overnight regression to fail

### CSRCompiler Generates:

- UVM register class definitions – CSRCompiler generates the UVM SystemVerilog class definitions for the control and status registers based on the UVM register package. The register and its UVM class definition are always in sync
- Improved backdoor access for VMM – CSRCompiler has capabilities beyond those of RALF/ralgen for specifying HDL paths
- Conversion from VMM RALF – Semifore offers a conversion facility to translate VMM RALF files into CSRSpec, SystemRDL, IP-XACT, or spreadsheets. This allows for easy import of legacy designs
- Verilog and VHDL header files – automatically generated, extensive set of Verilog macro or VHDL constraint definitions, indispensable for verifying the DUT. This ensures the verification team is always accessing the most up-to-date configuration and status register information

### Advanced CSRCompiler Features

CSRCompiler's advanced features provide numerous benefits over homegrown scripts. These scripts often fall short in providing accurate, complete and consistently generated views of your large address map; views that are critical to all members of your team.

| Feature | CSRCompiler | Homegrown scripts |
|---|---|---|
| Field / register cross referencing | ✓ | x |
| Time-saving template support | ✓ | x |
| Industry-standard buses | ✓ | x |
| Detects faulty 3rd-party IP cores | ✓ | x |
| Extensive error / syntax checking | ✓ | x |
| IEEE IP-XACT semantic consistency rule checks | ✓ | x |
| Hardware interrupt bit-enable support | ✓ | x |
| All features QA'd against large regression test suite | ✓ | ? |
| Single source for generating RTL, DV, firmware & documentation | ✓ | x |
| UVM, OVM, VMM register class definitions | ✓ | x |
| Improved backdoor access for VMM | ✓ | x |
| Multiple domains support | ✓ | x |
| Large capacity (100,000 registers) | ✓ | ? |
| High-speed (38sec / 10,000 registers) | ✓ | x |
| Virtual register files | ✓ | x |

## Contact us for an evaluation

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